

IN THE CLAIMS

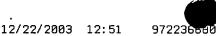
This listing of claims will replace all prior versions, and listings, of claims in the application:

- 1. (currently amended): A graphics accelerator, comprising:
 - a plurality of specialized processing subunits, interconnected through a serial message-passing interface to provide a generally pipelined graphics accelerator architecture; and
 - a memory interface which provides a high bandwidth interface independent of said serial message-passing interface directly to a local buffer memory associated with said graphics accelerator, said memory capable of storing displayable pixel information.
- 2. (original): The accelerator of Claim 1, wherein ones of said subunits are configured so that said memory interface accesses multiple tiles of pixels simultaneously.





- 3. (currently amended): A graphics accelerator, comprising:
 - a plurality of specialized processing subunits,
 - interconnected through a serial message-passing interface to provide a reconfigurably pipelined graphics accelerator architecture;
 - at least one of said specialized processing subunits comprising multiple subprocessors connected to operate in parallel on separate tasks; and
 - a high bandwidth memory interface independent of said serial messagepassing interface which interfaces to local buffer a memory of said graphics accelerator, said memory capable of storing displayable pixel information;
 - wherein said serial interface also permits downloading of image data to ones of said subunits.
- 4. (currently amended): The accelerator of Claim [[1]]3, wherein ones of said subunits are configured so that said memory interface accesses multiple tiles of pixels simultaneously.
- The accelerator of Claim 3, wherein ones of said subunits are 5. (new): configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.
- The accelerator of Claim 3, wherein said subunits include a 6. (new): currnet parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.



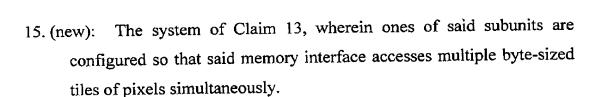
The accelerator of Claim 1, wherein ones of said subunits are 7. (new): configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.



- The accelerator of Claim 1, wherein said subunits include a 8. (new): currnet parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.
- A graphics rendering system comprising: 9. (new):
 - a host processor;
 - a system memory; and
 - a graphics accelerator comprising:
 - a plurality of specialized processing subunits, interconnected through a message-passing interface to provide a generally pipelined graphics accelerator architecture; and
 - a memory interface which provides a high bandwidth interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator, said memory capable of storing displayable pixel information.
- The system of Claim 9, wherein ones of said subunits are 10. (new): configured so that said memory interface accesses multiple tiles of pixels simultaneously.
- The system of Claim 9, wherein ones of said subunits are 11. (new): configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.



- The system of Claim 9, wherein said subunits include a currnet 12. (new): parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.
- A graphics rendering system comprising: 13. (new):
 - a host processor;
 - a system memory; and
 - a graphics accelerator comprising:
 - a plurality of specialized processing subunits,
 - interconnected through a serial message-passing interface to provide a reconfigurably pipelined graphics accelerator architecture;
 - at least one of said specialized processing subunits comprising multiple subprocessors connected to operate in parallel on separate tasks; and
 - a high bandwidth memory interface independent of said serial message-passing interface which interfaces to a memory of said graphics accelerator, said memory capable of storing displayable pixel information;
 - wherein said serial interface also permits downloading of image data to ones of said subunits.
- The system of Claim 13, wherein ones of said subunits are 14. (new): configured so that said memory interface accesses multiple tiles of pixels simultaneously.





- The system of Claim 13, wherein said subunits include a currnet 16. (new): parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.
- A computing system for graphics rendering, the system 17. (new): comprising:
 - a host processor;
 - a system memory; and
 - a computer graphics pipeline coupled to said host processor; the computer graphics pipeline comprising:
 - a plurality of specialized processing subunits, interconnected through a serial message-passing interface to provide a generally pipelined graphics accelerator architecture; and
 - a memory interface which provides a high bandwidth interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator, said memory capable of storing displayable pixel information.
- The system of Claim 17, wherein ones of said subunits are 18. (new): configured so that said memory interface accesses multiple tiles of pixels simultaneously.

- The system of Claim 17, wherein ones of said subunits are 19. (new): configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.
- The system of Claim 17, wherein said subunits include a currnet 20. (new): parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.
- A computing system for graphics rendering, the system 21. (new): comprising:
 - a host processor;
 - a system memory; and
 - a computer graphics pipeline coupled to said host processor; the computer graphics pipeline comprising:
 - a plurality of specialized processing subunits,
 - interconnected through a serial message-passing interface to provide a reconfigurably pipelined graphics accelerator architecture;
 - at least one of said specialized processing subunits comprising multiple subprocessors connected to operate in parallel on separate tasks; and
 - a high bandwidth memory interface independent of said serial message-passing interface which interfaces to a memory of said graphics accelerator, said memory capable of storing displayable pixel information;
 - wherein said serial interface also permits downloading of image data to ones of said subunits.

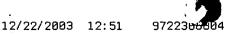


- The method of Claim 25, wherein ones of said subunits are 27. (new): configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.
- The method of Claim 25, wherein said subunits include a currnet 28. (new): parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.
- A method of designing graphics accelerators, comprising the 29. (new): steps of:
 - interconnecting a plurality of specialized processing subunits through a serial message-passing interface to provide a reconfigurably pipelined graphics accelerator;
 - at least one of said specialized processing subunits comprising multiple subprocessors connected to operate in parallel on separate tasks; and
 - providing a interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator through a memory interface, said memory capable of storing displayable pixel information;
 - wherein said serial interface also permits downloading of image data to ones of said subunits.
- The method of Claim 29, wherein ones of said subunits are 30. (new): configured so that said memory interface accesses multiple tiles of pixels simultaneously.



- 22. (new): The system of Claim 21, wherein ones of said subunits are configured so that said memory interface accesses multiple tiles of pixels simultaneously.
- The system of Claim 21, wherein ones of said subunits are 23. (new): configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.
- The system of Claim 21, wherein said subunits include a currnet 24. (new): parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.
- A method of designing graphics accelerators, comprising the 25. (new): steps of:
 - interconnecting a plurality of specialized processing subunits through a serial message-passing interface to provide a generally pipelined graphics accelerator; and
 - providing a high bandwidth interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator through a memory interface, said memory capable of storing displayable pixel information.
- The method of Claim 25, wherein ones of said subunits are 26. (new): configured so that said memory interface accesses multiple tiles of pixels simultaneously.

- The method of Claim 29, wherein ones of said subunits are 31. (new): configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.
- The method of Claim 29, wherein said subunits include a currnet 32. (new): parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.
- A graphics rendering method, comprising the steps of: 33. (new): receiving graphics primitives; and sending said graphics primitives through a graphics accelerator comprising: a plurality of specialized processing subunits, interconnected through
 - a serial message-passing interface to provide a generally pipelined architecture; and
 - a memory interface which provides a high bandwidth interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator, said memory capable of storing displayable pixel information.
- The method of Claim 33, wherein ones of said subunits are 34. (new): configured so that said memory interface accesses multiple tiles of pixels simultaneously.
- The method of Claim 33, wherein ones of said subunits are 35. (new): configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.



The method of Claim 33, wherein said subunits include a currnet 36. (new): parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.



- A graphics rendering method, comprising the steps of: 37. (new): receiving graphics primitives; and
 - sending said graphics primitives through a graphics accelerator comprising:
 - a plurality of specialized processing subunits,
 - interconnected through a serial message-passing interface to provide a reconfigurably pipelined graphics accelerator architecture;
 - at least one of said specialized processing subunits comprising multiple subprocessors connected to operate in parallel on separate tasks; and
 - a high bandwidth memory interface independent of said serial message-passing interface which interfaces directly to a memory of said graphics accelerator, said memory capable of storing displayable pixel information;
 - wherein said serial interface also permits downloading of image data to ones of said subunits.
- The method of Claim 37, wherein ones of said subunits are 38. (new): configured so that said memory interface accesses multiple tiles of pixels simultaneously.



The method of Claim 37, wherein ones of said subunits are configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.



The method of Claim 37, wherein said subunits include a currnet 40. (new): parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.